

REMARKS/ARGUMENTS

The Applicant respectfully requests further examination and reconsideration in view of the amendments above and the comments set forth fully below. Claims 1-3, 5, 8, 9, and 37-39 were pending. Within the Office Action mailed May 9, 2011 (hereafter “Office Action”), Claims 1-3, 8, 9, and 37-39 have been rejected. Claim 5 is objected to. By the above amendment, Claims 1 and 8 are amended. Accordingly, Claims 1-3, 5, 8, 9, and 37-39 are currently pending in the application.

Advisory Action

Within the Advisory Action mailed July 29, 2011, the Examiner states that the present specification indicates at Figure 2, element 256 and Figure 5, element 554, that there is only one output programming line (element 256, 554) from the serial control and that this is analogous to the Applicant’s argument that McCarthy teaches a single programmable input line 191. The Applicant respectfully submits that the Examiner has mis-characterized the teachings of the serial control element in Figures 2 and 5. Serial control 256 is shown Figure 2 as having input 258 and output 260. However, this is merely representative of general input and output signaling. In fact, the description on page 5, lines 11-12 indicates that the output line 260 is representative of general output functionality, “control circuitry 256 controls phased locked loops PLL1 and PLL2 to set frequencies of local oscillators LO1 264 and LO2 268.” Further, Figure 4 shows serial test and fix control unit 428 as providing multiple signal lines to control elements 418-426. The Examiner has applied physical structure, a single output line, where no such teaching is indicated. In contrast, McCarthy specifically teaches in paragraphs 0014 and 0021 that a single signal at line 191 is used to control each of the capacitive circuits 110, 115, 120.

Further, the present specification specifically teaches that each switched capacitor 306-314 are each independently set by transistors 324, 330, 336, 342, 348, respectively, and that transistors 324, 330, 336, 342, 348 are controlled by control lines 408-416, respectively. [Present Specification, paragraph 0053] Each of the control lines 408-416 is independently controlled by programmable storage locations. [Present Specification, paragraph 0057]

Claim Amendments

By the above amendment, Claim 1 is amended such that the first filter stage further includes a first adjustable capacitor array having a first plurality of switches coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of the first plurality of switches controlled by a first plurality of programmable data

storage locations. Support for this amendment is found at least in Figure 3, transistors 324, 330, 336, 342, 348, paragraphs 0050, 0053, 0057.

By the above amendment, Claim 8 is amended to replace “a first plurality of fuses” with “a first plurality of programmable data storage locations.” Support for this amendment is found in claim 1 which includes “the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of programmable data storage locations, the first plurality of programmable data storage locations programmable through a serial control interface”.

Rejections Under 35 U.S.C. §103:

Within the Office Action, Claims 1-3, 8, 9, and 37-39 have been rejected as being unpatentable over US Patent Application Publication No. 2004/0116096 to Shen (hereinafter “Shen”) in view of US Patent Application Publication No. 2003/0193373 to McCarthy et al. (hereinafter “McCarthy”) and further in view of US Patent No. 6,014,554 to Smith (hereinafter “Smith”). Applicant respectfully disagrees.

Shen teaches an RF communications receiver which permits greater integration on standard silicon chips and consumes less power than previous receivers. Also, Shen teaches a new method for using a tracking polyphase filter for image rejection of variable intermediate frequencies, wherein the method allows for reduced sensitivity to resistor and capacitor manufacturing variations and allows for the polyphase filter response to be enhanced compared to the prior art. [Shen, Abstract]

McCarthy teaches a programmable capacitive network for use in a tunable resonant circuit that is particularly useful in the tuning of a voltage controlled oscillator formed on a substrate, such as a semiconductor substrate or the like. The programmable capacitive network includes a plurality of capacitive elements. An interconnected network of voltage gate elements and fuse elements are interconnected with the capacitive elements to selectively connect one or more of the plurality of capacitive elements in the resonant circuit in response to at least one program control signal. In accordance with one embodiment, the voltage gate elements are diodes. [McCarthy, Abstract]

Smith teaches a method and apparatus for tuning an analog filter that is embodied in a larger circuit in which the analog input signal to the filter is, at some point prior to the filter, in digital form. The digital version of the input signal to the filter is stored in memory. The output signal from the filter corresponding to the stored input signal is digitized and compared to the stored digital input signal to the filter. Based on the known input signal and the known desired frequency characteristics of the filter, the desired output signal is a known quantity. If the actual

output signal differs from the expected output signal, the filter is tuned accordingly. The process may be performed continually on all input data or on discrete sections of the input data. [Smith, Abstract]

As admitted to in the Office Action, Shen does not disclose a programmable filter with an arrangement as claimed. Instead, McCarthy is cited as teaching a first filter stage, the first filter stage including a first LC resonator and including a first adjustable capacitor array coupled to the first LC resonator. [Office Action, pages 2-3] It is further admitted to in the Office Action that the modified programmable filter of Shen and McCarthy disclose that the capacitor switching matrix can be programmed to select a capacitor to enable/disable but not explicitly disclose that the capacitor matrix can be programmed by data storage location. Instead, Smith is cited as disclosing a capacitor matrix that can be programmed by data storage location. [Office Action, page 3] The Applicant respectfully submits that the proposed combination does not teach the limitations as claimed.

Further, Claim 1 is amended to specify that the adjustable capacitor array includes a plurality of switches, and that the switches are controlled by programmable data storage locations. McCarthy is cited as teaching the claimed adjustable capacitor array. However, the capacitive network taught by McCarthy does not includes switches.

Claim 1 is directed to an intermediate frequency filter for use in an integrated circuit, comprising a first filter stage, the first filter stage including a first LC resonator, and the first filter stage further including a first adjustable capacitor array having a first plurality of switches coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of the first plurality of switches controlled by a first plurality of programmable data storage locations, the first plurality of programmable data storage locations programmable through a serial control interface..

In contrast, McCarthy teaches that the capacitive elements 110, 115, 120 in Figures 1A and 1B, and capacitive elements 202-212 in Figure 2, are adjusted through the use of a single programmable input line 191. [McCarthy, paragraph 14 and 21, Figures 1A, 1B, 2] Further, McCarthy fails to teach a capacitive network that includes switches.

Even if it is proper to apply programming via data storage locations of Smith, as proposed, only a single programming line 191 of McCarthy is available such that only a single programmable data storage location is used to adjust the capacitive elements. This is not the same as the claimed limitations which specify that the capacitive array is adjustable through use of a plurality of programmable data storage elements, not a single programmable data storage element. As such, the proposed combination of Shen, McCarthy, and Smith does not teach the limitations of Claim 1. Claims 2, 3, 5, and 37-39 are dependent upon the allowable Claim 1 and

are therefore similarly allowable.

Claim 8 is directed toward a circuit formed as part of a single integrated circuit, the circuit comprising a first amplifier, a first oscillator, a first mixer coupled to the first amplifier and the first oscillator, a second oscillator, a second mixer coupled to the second oscillator, a second amplifier coupled to the second mixer, a serial control module, an intermediate frequency filter (IF filter), the IF filter including a first filter stage, the first filter stage including a first LC resonator, the first filter stage further including a first adjustable capacitor array coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of programmable data storage locations, the first plurality of programmable data storage locations programmable through the serial control module, and wherein the second mixer is coupled to the IF filter and the IF filter is coupled to the first mixer. For at least the same reasons as those described above in regard to Claim 1, the independent Claim 8 is allowable over Shen in view of McCarthy in view of Smith. Claim 9 is dependent upon the allowable Claim 8, and is therefore similarly allowable.

Conclusion

The Applicant respectfully submits that the above claims are in a condition for allowance, and allowance at an early date would be appreciated. If the Examiner has any questions or comments, the Examiner is encouraged to call the undersigned at (408) 530-9700 to discuss them so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
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